As to this amendment, the specification and claims 1, 5-15, 17-18 and 20 have been amended. A marked up version of the amended specification and claims is attached hereto. Claims 21-52 have been added. Applicants respectfully submit that all of the pending claims (1-52) are patentable without further amendment. Accordingly, Applicants respectfully request reconsideration, removal of the rejection, and allowance of all of the claims.

Telephone Interview With Examiner Phan

As stated above, Applicants appreciate the courtesy extended by Examiner Phan in telephone interviews on October 8, 2001 and October 9, 2001. In the telephone interviews, Examiner Phan provided further details in regard to the rejection of claims 1 and 5. No agreement was reached.

Claim 1

In regard to claim 1, Examiner Phan stated that U.S. Pat No. 6,169,747 issued to Sartain et al. (hereafter Sartain et al.) shows three data streams (A, B, C) that can be viewed collectively as a multi-bit digital signal. The Examiner further stated that the one-bit DACs (DAC 29 of the DAC 10A, the DAC 29 of the DAC 10B, and the DAC 29 of the DAC 10N) can be viewed collectively as a DAC that outputs at least two analog signals each indicative of a sum of values of bits in the multi-bit digital signal. In support of the latter statement, the Examiner stated that each of the one-bit DACs outputs a signal in response to its data stream, which is in turn part of the multi-bit digital signal and, therefore, each output must be indicative of a sum of values of bits in the multi-bit digital signal.

Lastly, the Examiner stated that the SC filters 21 (SC filter 21 of the DAC 10A, the SC filter 21 of the DAC 10B, and the SC filter 21 of the DAC 10N), can be viewed collectively as a signal conditioning stage that receives at least two of the at least two analog signals.

Claim 5

In regard to claim 5, Examiner Phan stated that FIG. 5 of Sartain et al. shows a DAC system that receives digital input signals at an input rate and outputs analog signals at an output rate different than the input rate. The Examiner stated that the output rate must be different than the input rate because the DAC system includes an interpolation filter (citing col. 4, lines 30-32).

Objection to the Specification

Paragraph 1 of the Office Action objects to the specification. The Office Action states that the detailed description does not describe FIG. 32.

Applicants respectfully disagree. FIG. 32 shows an example of a 3-phase clock that may be used in the operation of the squaring circuit of FIG. 31. Applicants admit that these exact words do not appear in the description. Nonetheless, FIG. 32 is adequately described to one of ordinary skill in the art. FIG. 32 and FIG. 31 appear on one drawing sheet. FIG. 32 clearly shows an example of a 3-phase clock, and FIG. 31, which shows one embodiment of a squaring circuit, clearly calls for a 3-phase clock. Moreover, in describing the operation of the squaring circuit of FIG. 31, the description refers to "the 3-phase clock", "the three clock phases", "on P1", "on P2 of the 3-phase clock", "on phase P3 of the 3-phase clock"(see page 32, lines 6, 10, 14, 20, 31 and page 33, line 8). There are no other figures on the drawing sheet.

Nevertheless, in order to further prosecution, the detailed description has been amended as required. No new matter has been added. Reconsideration and removal of the grounds for objection to the specification is hereby respectfully requested.

Claim Amendments and Added Claims

Claims 1, 5-15, 17-18, and 19 have been amended to clarify these claims. Claims 21-52 have been added. The specification provides support for the amendments and the new claims, at least, for example, at one or more portions of FIG. 27, and one or more portions of page 27, line 14 – page 28, line 30. No new matter has been added.

Claim Rejections Under 35 U.S.C. 102

In paragraph 3, the Office Action rejects claims 1-20 under 35 U.S.C. 102(e) as being anticipated by Sartain et al.

The Office Action states that FIG. 2 of Sartain et al. discloses a prior art multi-bit DAC system comprising a plurality of DACs 29, and a plurality of switch capacitor filters 21.

Further details were provided in the telephone interviews of October 8, 2001 and October 9, 2001, as discussed above.

Claims 1-4 and 21-28 and 49-51

Applicants traverse the rejection of claim 1, as amended.

Claim 1, as amended, recites a system comprising a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of said bits in the multi-bit digital signal. The DAC further includes a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal.

FIG. 2 (FIGS. 2A and 2B) of Sartain et al. shows a multistreamed DAC system which receives data streams A-N. The multistream DAC system is made up of a plurality of DAC systems 10A-10N. Each DAC system receives a respective one of the data streams, converts its data stream into a one bit data stream, and sends the one bit data stream to its one-bit DAC 29. Each DAC has a filter 17 that receives the signal from its one bit DAC 29.

Thus, Sartain et al. teaches that each of the one-bit DACs 29 receives its own data stream and outputs an analog signal based on that data stream.

Consequently, even if the data streams A-N constitute a multi-bit digital signal, and even if the three DACs 29 (the DAC 29 of the DAC 10A, the DAC 29 of the DAC 10B, and the DAC 29 of the DAC 10C) constitute a single DAC (as asserted by the Examiner in the telephone interviews of October 8-9), which Applicants do not admit, the latter-mentioned DAC does not output at least two analog signals including **a first analog signal indicative of a sum of values of bits** in the multi-bit digital signal**, and a second analog signal also indicative of said sum of values of said bits** in the multi-bit digital signal, as recited in claim 1 (emphasis added).

Therefore, Sartain et al. cannot teach or suggest a system comprising: a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, **the first analog signal being indicative of a sum of values of bits** in the multi-bit digital signal**, the second analog signal also being indicative of said sum of values of said bits** in the multi-bit digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal, as recited in claim 1 (emphasis added).

Accordingly, reconsideration and allowance of claim 1, as amended, is respectfully requested.

Because the above reasons are sufficient to traverse the rejection, Applicants do not address other possible reasons for traversing the rejection.

Claims 2-4, 21-28, and 49-51 depend from claim 1 and are patentable for at least the same reasons as stated above for claim 1. Reconsideration and allowance of claims 2-4 and 21-28, and 49-51 is respectfully requested.

In addition, Applicants point out that claim 27 further recites that the signal conditioning stage generates **a signal that is responsive to both the first analog signal and the second analog signal** (emphasis added). This is neither taught nor suggested by Sartain et al. Instead, Sartain et al. teaches that each of the SC filters 17 (the SC filter 17 of the DAC 10A, the SC filter 17 of the DAC 10B, and the SC filter 17 of the DAC 10N) receives a different input signal and outputs a signal responsive only thereto (i.e., the SC filter 17 of the DAC 10A receives outputs the signal that is indicative of the bits in the data stream A, the DAC 29 of the DAC 10B outputs a signal that is indicative of the bits in the data stream B, and the DAC 29 of the DAC 10C outputs a signal that is indicative of the bits in the data stream C). Consequently, even if the SC filters 17 (the SC filter 17 of the DAC 10A, the SC filter 17 of the DAC 10B, and the SC filter 17 of the DAC 10N) constitute a signal conditioning stage, as asserted by the Examiner, the asserted signal conditioning stage does not **generate a signal that is responsive to both the first analog signal and the second analog signal**, as recited in claim 27 (emphasis added).

In addition, claim 28 further recites that the signal conditioning stage generates **a signal that is responsive to each of the at least two of the at least two analog signals,** (emphasis added). As stated above with respect to claim 27, Sartain does not teach or suggest a signal conditioning stage that generates a signal that is responsive to both the first analog signal and the second analog signal (emphasis added). Consequently, Sartain et al. cannot teach or suggest a signal conditioning stage that generates a signal that is **responsive to each of the at least two of the at least two analog signals**, as recited in claim 28 (emphasis added).

In addition, claims 49-51 recite that the DAC comprises **a switched capacitor network including at least two capacitors that share charge** with one another, the first analog signal and the second analog signal comprising charge supplied from the at least two capacitors (emphasis added). Sartain does not teach or suggest such a DAC.

Claims 5-12 and 52

The Office Action does not provide any rationale for the rejection of claim 5. Details regarding the rejection were provided in the telephone interviews of October 8, 2001 and October 9, 2001, discussed above.

Applicants traverse the rejection of claim 5, as amended.

Claim 5, as amended, recites a system comprising a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals to a signal conditioning stage at an output data rate, each of the analog signals being indicative of an associated one of the digital input signals, the magnitude of the output data rate being different than the magnitude of the input data rate, wherein more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

FIG. 5 of Sartain et al. shows a DAC system including an interpolation filter, a modulator and a one-bit DAC 129.

However, it would appear that **only one analog signal is generated during a digital to analog conversion cycle**.

Consequently, even if FIG. 5 of Sartain et al. discloses a DAC that receives digital input signals at an input rate and outputs analog signals at an output rate different than the input rate (as asserted by the Examiner in the telephone interviews of October 8-9), which Applicants do not admit, the DAC does not generate more than one of the analog signals during a **single digital to analog conversion cycle** of the DAC, as recited in claim 5, as amended (emphasis added).

Therefore, Sartain et al. cannot teach or suggest a system comprising a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals to a signal conditioning stage at an output data rate, each of the analog samples being indicative of an associated one of the digital input signals, the magnitude of the output data rate being different than the magnitude of the input data rate, wherein **more than one of the analog signals is generated during a single digital to analog conversion cycle** of the DAC, as recited in claim 5 (emphasis added).

Accordingly, reconsideration and allowance of claim 5, as amended, is respectfully requested.

Because the above reasons are sufficient to traverse the rejection, Applicants do not address other possible reasons for traversing the rejection.

Claims 6-12 and 52 depend from claim 5 and are patentable for at least the same reasons as stated above for claim 5. Reconsideration and allowance of claims 6-12 and 52 is hereby respectfully requested.

In addition, claim 52 recites that the DAC comprises a switched capacitor network and that more than one of the analog signals is generated during a single digital to analog conversion cycle of the switched capacitor network. Sartain et al. does not teach or suggest such a feature.

Claims 13-16 and 37-38

Applicants respectfully traverse the rejection of claim 13, as amended.

Claim 13, as amended, recites a method comprising: receiving a multi-bit digital signal; generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and filtering at least two of the at least two analog output signals, including the first analog signal and the second analog signal.

Sartain et al. does not teach or suggest generating **a first analog signal that is indicative of a sum of values of bits** in a multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal.

Consequently, Sartain et al. does not teach or suggest a method comprising: receiving a multi-bit digital signal; generating at least two analog signals including **a first analog signal that is indicative of a sum of values of bits** in the multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal; and filtering at least two of the at least two analog output signals, including the first analog signal and the second analog signal, as recited in claim 13, as amended (emphasis added).

Accordingly, reconsideration and allowance of claim 13, as amended, is respectfully requested.

Because the above reasons are sufficient to traverse the rejection, Applicants do not address other possible reasons for traversing the rejection.

Claims 14-16 and 37-38 depend from claim 13 and are patentable for at least the same reasons as stated above for claim 13. Reconsideration and allowance of claims 14-16 and 37-38 is hereby respectfully requested.

In addition, claim 37 recites generating **a signal that is responsive to both the first analog signal and the second analog signal** (emphasis added). Claim 38 recites generating **a signal that is responsive to each of the at least two of the at least two analog signals,** (emphasis added). Neither of these features is taught or suggested by Sartain et al.

Claims 17 –20 and 47-48

Applicants respectfully traverse the rejection of claim 17, as amended.

Claim 17, as amended, recites a system comprising: means for receiving a multi-bit digital signal; means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and means for filtering at least two of the at least two analog signals, including the first analog signal and the second analog signal.

As stated above for claim 13, Sartain et al. does not teach or suggest generating **a first analog signal that is indicative of a sum of values of bits** in a multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal.

Consequently, Sartain et al cannot teach or suggest a system comprising: means for receiving a multi-bit digital signal; means for generating at least two analog signals including a **first analog signal that is indicative of a sum of values of bits** in the multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal; and means for filtering at least two of the at least two analog signals, including the first analog signal and the second analog signal, as recited in claim 17, as amended (emphasis added).

Accordingly, reconsideration and allowance of claim 17, as amended, is respectfully requested.

Because the above reasons are sufficient to traverse the rejection, Applicants do not address other possible reasons for traversing the rejection.

Claims 18-20 and 47-48 depend from claim 17 and are patentable for at least the same reasons as stated above for claim 17. Reconsideration and allowance of claims 18-20 and 47-48 is hereby respectfully requested.

In addition, claim 47 recites that the signal conditioning stage generates **a signal that is responsive to both the first analog signal and the second analog signal** (emphasis added). Claim 48 further recites that the signal conditioning stage generates **a signal that is responsive to each of the at least two of the at least two analog signals,** (emphasis added). As stated above for claims 27-28, neither of these features is taught or suggested by Sartain et al.

Discussion of New Independent Claims and Claims Depending Therefrom

Claim 29 is an independent claim that recites a method comprising: receiving a multi-bit digital signal; generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal.

As stated above for claim 13, Sartain et al. does not teach or suggest generating **a first analog signal that is indicative of a sum of values of bits** in a multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal.

Consequently, Sartain et al. cannot teach or suggest a method comprising: receiving a multi-bit digital signal; generating at least two analog signals including **a first analog signal that is indicative of a sum of values of bits** in the multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal; and providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal, as recited in claim 29 (emphasis added).

Accordingly, allowance of claim 29 is requested.

Claims 30-38 depend from claim 29 and are patentable for at least the same reasons as stated above for claim 29. Accordingly allowance of claims 30-38 is hereby respectfully requested.

In addition, claim 37 recites generating **a signal that is responsive to both the first analog signal and the second analog signal** (emphasis added). Claim 38 recites generating **a signal that is responsive to each of the at least two of the at least two analog signals,**

(emphasis added). As stated above for claims 27-28, neither of these features is taught or suggested by Sartain et al.

Claim 39 is an independent claim that recites a system comprising: means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital input signal and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal.

As stated above for claim 13, Sartain et al. does not teach or suggest generating **a first analog signal that is indicative of a sum of values of bits** in a multi-bit digital signal, **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal.

Consequently, Sartain et al. cannot teach or suggest a system comprising: means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including **a first analog signal that is indicative of a sum of values of bits** in the multi-bit digital input signal **and a second analog signal that is indicative of said sum of values of said bits** in the multi-bit digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal, as recited in claim 39 (emphasis added).

Accordingly, allowance of claim 39 is requested.

Claims 40-48 depend from claim 39 and are patentable for at least the same reasons as stated above for claim 39. Accordingly allowance of claims 40-48 is hereby respectfully requested.

In addition, claim 47 recites that the signal conditioning stage generates **a signal that is responsive to both the first analog signal and the second analog signal** (emphasis added). Claim 48 further recites that the signal conditioning stage generates **a signal that is responsive to each of the at least two of the at least two analog signals,** (emphasis added). As stated above for claims 27-28, neither of these features is taught or suggested by Sartain et al.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Ferguson et al., Applicant

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Date: November ____, 2001
x12/13/01x

MARKED-UP SPECIFICATION

Please amend the paragraph beginning on page 9, line 20 to read as follows:

FIG. 32 shows a three phase clock [is a block diagram of one embodiment of a squaring circuit];

Please amend the paragraph beginning on page 32, line 5 to read as follows:

FIGS. 33A-33C are block diagrams showing the operation of the squaring circuit 500 of FIG. 31 for each of the three clock phases (see FIG. 32) in the event that input terminals 512, 514, 516, 518 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 0, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of the 3-phase clock (FIG. 32), all of the charge sharing switches S200, S201, S202, and S203 and the output switch S204, are in the open condition. The capacitor C1 is charged to V_{ref} in response to the logic state 1 on terminal 512. Capacitors C2, C3 and C4 are all discharged to ground in response to the logic state 0 signals on terminals 514,516,518, respectively. Referring now to FIG. 33B, on phase P1 of the 3-phase clock (FIG. 32) all of the charging switches S3, S6, S9 and S12 (FIG. 31) and the output switch S204 are in an open condition, and all of the charge sharing switches S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/4$. Referring now to FIG. 33C, on P2 of the 3-phase clock (FIG. 32) switch S200 is in the closed condition because P2 has a logic 1 state and bit_1 has a logic state 1. Switches S201, S202, S203 are in the open condition because bit_2, bit_3, bit_4, have a logic state 0. Output switch S204 is in the closed condition, and capacitor C1 (FIG. 31) of one-bit DAC 162 delivers its charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to C*Vref/4.

Please amend the paragraph beginning on page 32, line 26 to read as follows:

FIGS. 34A-34C are block diagrams showing the operation of the squaring circuit 500 of FIG. 31 for each of the 3 clock phases in the event that input terminals 512, 514, 516, 518 are

supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 1, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of the 3-phase clock (FIG. 32), all of the charge sharing switches S200, S201, S202, and S203 and the output switch S204, are in the open condition. The capacitor C1 and the capacitor are each charged to V_{ref} in response to the logic state 1 on terminal 512 and 514, respectively. Capacitors C3 and C4 are all discharged to ground in response to the logic 0 signals on terminals 516, 518, respectively. Referring now to FIG. 34B, on phase P1, all of the charging switches S3, S6, S9 and S12 (FIG. 31) and the output switch S204 are in an open condition, and all of the charge sharing switches S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/2$. Referring now to FIG. 33C, on[l] phase P2 of the 3-phase clock (FIG. 32), switch S200 is in the closed condition because P2 has a logic state 1 and bit_1 has a logic state 1. Switch S201 is in the closed condition because P2 has a logic state 1 and bit_2 has a logic state 1. Switches S202, S203 are in the open condition because bit_3, bit_4, have a logic state 0. Output switch S204 is in the closed condition, and capacitors C1 and C2 (FIG. 31) of one-bit DACs 162, 164 delivers charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to C*Vref.

MARKED-UP CLAIMS

1. (Amended) A system comprising:

a DAC that receives a multi-bit digital signal and outputs at least two analog signals [each] including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of said bits in the multi-bit digital signal; and

a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal.

5. (Amended) A system comprising:

a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals [indicative of the digital signals] to a signal conditioning stage at an output data rate, each of the analog signals being indicative of an associated one of the digital input signals, the magnitude of the [at an] output data rate being different than the magnitude of the input data rate, wherein more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

6. (Amended) The system of claim [1] 5 wherein the signal conditioning stage comprises a switched capacitor filter stage.

7. (Amended) The system of claim [1] 5 wherein the DAC comprises a switched capacitor DAC.

8. (Amended) The system of claim [1] 5 wherein the magnitude of the output data rate of the DAC is at least twice the magnitude of the input data rate of the DAC.

9. (Amended) The system of claim [1] 5 wherein the magnitude of the output data rate of the DAC is two times the magnitude of the input data rate of the DAC.

10. (Amended) The system of claim [9] 5 wherein [the analog signals are substantially equal to each other] the signal conditioning stage generates a signal responsive to the sequence of analog signals.

11. (Amended) The system of claim [1] 5 wherein the DAC receives one digital input signal per operating cycle and the analog signals are output at a non periodic rate over the operating cycle.

12. (Amended) The system of claim 11 wherein the analog signals have a periodic effect on an output of the signal conditioning stage.

13. (Amended) A method comprising:

receiving a multi-bit digital signal ;

generating at least two analog [output] signals including a first analog signal that is [each] indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

filtering at least two of the at least two analog output signals, including the first analog signal and the second analog signal.

14. (Amended) The method of claim 13 wherein [generating comprises generating] the at least two analog [output] signals [that] are substantially equal to one another.

15. (Amended) The method of claim 13 wherein the filtering comprises [delivering] providing the at least two of the at least two analog [output] signals to a switched capacitor filter.

17. (Amended) A system comprising:

means for receiving a multi-bit digital signal ;

means for generating at least two analog [output] signals [each] including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

means for filtering at least two of the at least two analog [output] signals, including the first analog signal and the second analog signal.

18. (Amended) The system of claim 17 wherein the [means for generating comprises means for generating] at least two analog [output] signals [that] are substantially equal to one another.

20. (Amended) The system of claim 17 wherein the means for generating comprises a switched capacitor DAC.